REMARKS

Claims 1-11 are pending in the present application. Claims 7-11 have been rejected under 35 U.S.C. §102. Claims 1-11 remain pending in the present application.

Present Invention

An application specific integrated circuit (ASIC) is disclosed. The ASIC comprises a standard cell, the standard cell including a plurality of logic functions. The ASIC further includes at least one FPGA interconnect coupled to at least a portion of the logic functions. The FPGA interconnect can be configured to select a particular logic function of the plurality of logic functions.

An ASIC in accordance with the present invention allows "field selection" of functions that are connected to the internal bus(es) and to external I/O. The functional block connections made with internal buses can be significantly wider and faster than buses brought on chip via external chip I/Os. Further, the ASIC reduces cost because selective bus connections can be made internal to the chip, thus eliminating the need for additional external pins. Finally, the ASIC reduces the cost of the packaged component by allowing the chip to be packaged in a lower pin count package.

Rejection Under 35 U.S.C. §102

The Examiner States:

> **Claims 1-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Lien et al. (US 6,211,697 B1).**
>
> **Regarding claims 1-7, Lien et al. discloses, in figure 11, an ASIC comprising:**

a standard cell (HA) including a plurality of logic functions (col. 4, lines 63+); a plurality of input output pins (col. 5, line 47); and at least one FPGA interconnect (see 48-56 in fig. 2) coupled to the plurality of I/O pins and the plurality of logic functions, wherein the at least one FPGA interconnect can be configured to select one of the plurality of logic functions (via lines G/2) utililizing field programming techniques (see IGs 26-34 and 58-100 in fig. 2); and wherein the one logic function is coupled to an internal bus (see 48-56 in fig. 2) via the at least one configured FPGA interconnect.

Regarding claims 8 and 9, utilizing at least one FPGA interconnect to correct wiring error which is a reversed bit order wiring error, when the ASIC is utilized on a printed circuit board, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987).

Regarding claims 10 and 11, Lien et al. discloses, in figure 9B, an ASIC comprising:

a plurality of I/O pins (col. 5, line 47);

a plurality of first logic functions (logic functions in HA 210) provided as part of a standard cell (HA 210-216);

a first FPGA interconnect (FPGA 218) coupled between the plurality of I/O pins and the plurality of first logic function, wherein the first FPGA interconnect can be configured to select at least one of the plurality of first logic functions (300 in Fig. 15 in combination with internal bus of FPGA 218, see fig. 2);

a bus (see 48-56 in Fig. 2; and 300 in Fig. 15) coupled to the plurality of first logic functions;

a second FPGA interconnect (FPGA 222) coupled between the bus and the plurality of first logic functions, wherein the second FPGA interconnect is configured to connect to one of the plurality of first logic functions to the bus (see col. 11, lines 23+); and

a plurality of second logic functions (HA 212) coupled to the bus.

<u>Applicant respectfully disagrees</u>

Lien et al. is directed to providing an integrated circuit (IC) that includes a field-programmable gate array (FPGA) and a hard array (HA). The FPGA is based on a specific

underlying logic and routing structure and includes a plurality of transistors and memory cells coupled to the specific underlying logic and routing structure for programming the specific underlying logic and routing structure. The HA is also based on the specific underlying logic and routing structure but it does not include transistors and memory cells coupled to the specific underlying logic and routing structure that are used for programming the specific underlying logic and routing structure.

Lien describes repeatedly throughout the patent that the purpose for the FPGA and HA to have the above-identified structure is to permit the same design software package to be used for programming FPGAs and for designing the HA. However, the FPGA interconnect as recited in the independent claims 1, 6 and 10 "can be configured to select ~~are~~ one of the plurality of logic functions" of the standard cell. There is no teaching or suggestion of such an interaction between the FPGA and HA of Lien et al.

Accordingly, applicant submits that independent claims 1, 6, and 10 are allowable for the above mentioned reason.

In addition, as to claims 8 and 9, since Lien et al. neither teaches or suggests a connection between the standard cell and the FPGA, there is no teaching suggestion that the FPGA can be utilized to correct a wiring error when the ASIC is utilized on a printed circuit board.

Applicant submits therefore, that claims 1-11 are allowable over the cited reference and respectfully requests reconsideration and allowance of the claims as now presented.

Applicant's attorney believes that this application is in condition for allowance. Should any unresolved issues remain, Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,

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Date

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